Known Good Die Testing of Wide S/C Band Power MMICs

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ABSTRACT

The testing process for power MMICs today is expensive and slow because it is done in a fixtured environment. The chip is usually diced up from a wafer, mounted on a carrier, and wire-bonded to an off-chip matching network (OCMN) before being tested. In this paper we demonstrate an integrated known-good-die testing solution at the wafer level, for a high-power S/C-band power amplifier. Fixtured and on-wafer results are compared.

INTRODUCTION

Power MMICs typically have very low output impedances. At relatively low frequencies, such as at S/C band, integrating the matching network on the chip becomes very expensive. Consequently, in practice, the matching network is built off-chip. As part of the testing process, wafers are diced up, individual chips are mounted on carriers together with OCMNs, and relevant wire-bond connections are made. Obviously, this is a very expensive testing scheme. In this paper, we propose an on-wafer testing solution by integrating the matching network in the membrane probe. Membrane probes [1,2] are well known for their applications to production probing. They are rugged, have the ability to withstand over a million contact cycles, and have better power bypassing than traditional needle cards. In this work, membrane probes were built to test a Lockheed Martin S/C band high power HBT chip [3] at the on-wafer level. The results are compared with fixtured measurements. The total output impedance of the chip is about 1.4 Ω and the input impedance is 50 Ω.

PROBE DESCRIPTION

The carrier level testing scenario is depicted in Figure 1. The diagram shows two OCMNs built on different substrates to keep within manufacturable dimensions. The larger OCMN has four inputs which are wire-bonded to the collector pads of the HBT chip. It has a dielectric constant of 50 to reduce the size of the low impedance microstrip lines. The smaller OCMN is printed on alumina to increase the width of the lines to facilitate fabrication. The matching network has passbands at S and C bands and a notch in between.

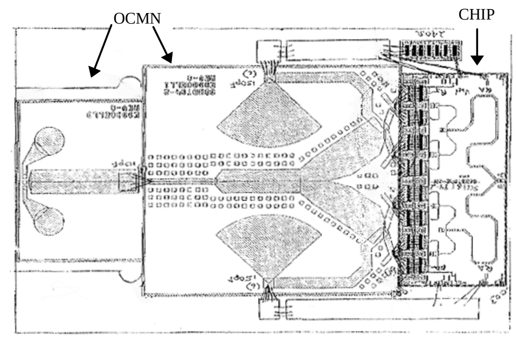

Figure 1: A carrier level testing proposition showing the two matching networks on different substrates wire-bonded to the HBT power amplifier collector pads.

Initially, as part of the membrane probe fabrication scheme, we attached the larger OCMN on the probe with epoxy and gold ribbons and integrated the smaller one in the membrane. The ground side of the OCMN laid against the probe and made contact with the meshed ground. Wide ribbons were attached from the top of the OCMN to the membrane signal lines. This design method did not work well, due to the large parasitics introduced through the ground structure which became intractable above 3 GHz. In addition, the epoxy resistance was not stable due to the small dimensions and mechanical stress, resulting in unsuitable bias conditions. Further reduction of parasitics would cause the OCMN to mechanically interfere with the chip as the membrane probe touched down on the wafer. Consequently, we decided to integrate circuitry of the larger OCMN into the membrane.

Integrating the OCMN into the probe posed some difficulty because of its relative size. The translated geometry is approximately 3 times larger, due to differences in the thickness and the dielectric constant of the OCMN and membrane.

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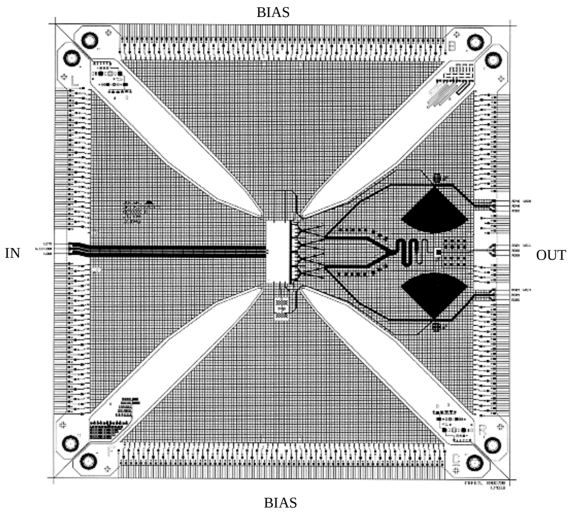

Figure 2: A membrane probe layout showing the input signal line on the left and the output circuit containing the matching network on the right. The bump footprint in the center matches that of the die shown in Figure 1.

Some sections of the matching network are meandered in order to fit it inside the 2" square LSI probe core as displayed in Figure 2. The entire output circuit is built with microstrip lines. The ground mesh is used to tie together the DC grounds and the RF lines. The bias lines are made sufficiently wide to carry high currents. The ground underneath the series DC blocking capacitor pad is removed to prevent any large parallel capacitive effect in that location. A wide ribbon, for purposes of low inductance, connects from the DC blocking capacitor to the matching network.

The input circuit is a 50-Ω CPW line, chosen for lower loss characteristics over microstrip lines. The skin-effect losses are dominant and, hence, CPW lines fare well due to larger geometries possible, all other parameters being equal. To prevent slot-line modes, parallel ground lines are constructed on the bottom layer which have via and bridge connections at regular intervals, as shown in Figure 2.

RESULTS

The output circuit of the probe was characterized using a custom impedance standard substrate (ISS), specifically designed for this probe. The probe was terminated in three known standards: a short, an open, and a load. From these three measurements and the assumption that $S_{12} = S_{21}$ from reciprocity, the three remaining S-parameters are calculated; they are exhibited in Figure 3. The S_{11}/S_{22} curves show that the matching network has a dual passband at S and C bands with a notch in the middle.

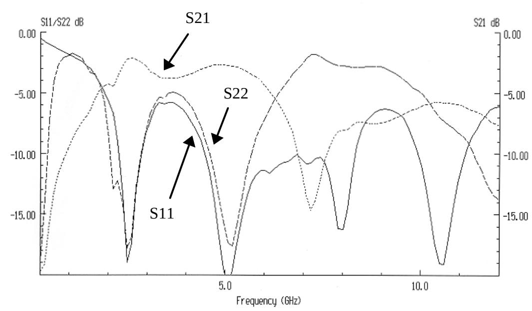

Figure 3: S-parameters of the S/C band membrane probe. The port 1 (chip side) reference impedance is 1.4 ohms real for this measurement. The calculated responses of S_{22} and S_{21} are not very valid beyond the 1-6 GHz frequency range because the low magnitude of S_{21} makes the extraction noisy.

Figure 4 compares the measured power level of the biased HBT chip using fixtured and on-wafer testing methods. The bias and input power levels are kept constant and the same chip is used for both tests. The two measured responses agree quite well up to 5 GHz, beyond which they start to differ appreciably. The differences seen at the lower frequency band are primarily due to the loss of the probe. They may also have been due to misalignment of ground pads that could have damaged one or two devices during testing.

To investigate the disparity seen at the higher frequency band, we simulated the membrane matching network and compared it with the OCMN. The impedance responses for the five-port network , displayed in Figure 5 on the Smith Chart, indicate that the matching network impedances become substantially different beyond 5 GHz. The responses have been made identical by adjusting the lengths of some sections of the probe matching network. We will incorporate this dimensional change in the next probe iteration to achieve identical response above 5 GHz. We will also extend this technology to test devices on-wafer at X- and Q-bands.

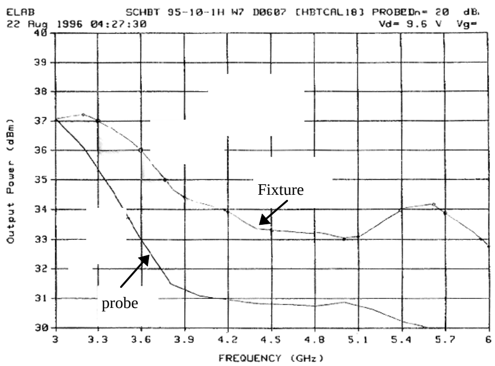

Figure 4: Comparison of measured responses between membrane probe and wire-bonded-on-carrier testing.

CONCLUSIONS

We have shown the viability of known good die testing at the wafer level using membrane probe technology which can integrate a matching network with an arbitrary response pattern over a wide band. This probing technology will allow lower costs, higher powers, and/or higher efficiencies in microwave power amplifiers, by making off-chip matching networks practical in manufacturing.

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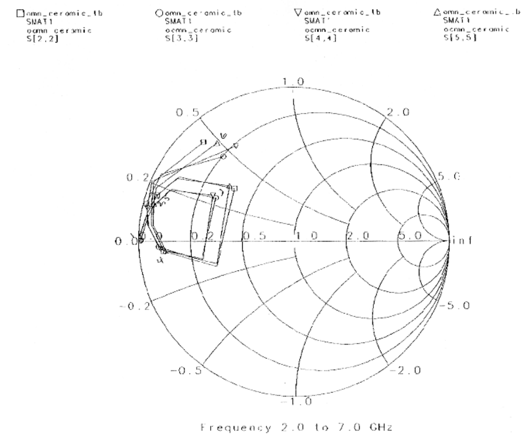

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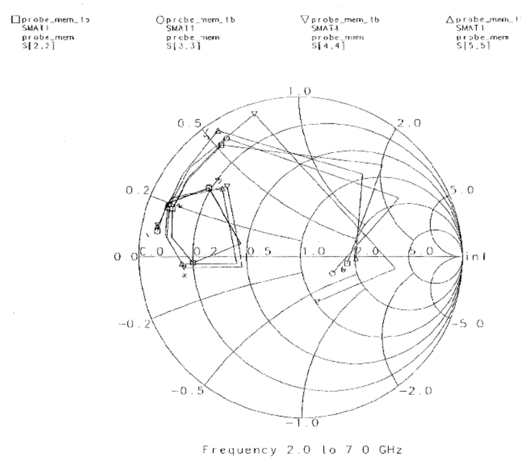

(b)

Figure 5: Comparison of simulated responses (S_{22}, S_{33}, S_{44}, and S_{55}) of (a) the OCMN and (b) the integrated membrane matching network showing their deviation starting around 5 GHz.